**SIKKIM INSTITUTE OF SCIENCE AND TECHNOLOGY**

**CHISOPANI, SOUTH SIKKIM**

**DEPARTMENT OF COMPUTER ENGINEERING**

**END SEMESTER EXAMINATION, B. TECH SEMESTER EXAMINATION -III**

Subject: -DIGITAL ELECTRONICS & LOGIC DESIGN LAB Subject Code: - BTCO-UG-L308

Time: - 2 hours Full Marks: - 50

**All the questions are compulsory and contains 2 Marks each**.

 1.A classification of integrated circuits with complexities of 30 to 300 equivalent gates on a single chip is known as?

1. VLSI
2. SSI
3. LSI
4. MSI

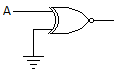
2.  2's complement of 1011011 is

1. 0100011
2. 0110101
3. 0100011
4. 0100101

3. DE Morgan’s Law states that

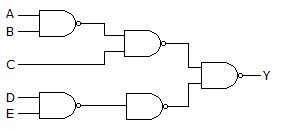
1. (A+B)' = A'\*B
2. (AB)' = A' + B'
3. (AB)' = A' + B
4. (AB)' = A + B

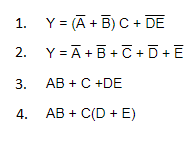
4.For the gate in the given figure the output will be ………..

[](https://electronicspost.com/wp-content/uploads/2016/04/mcq1.png)

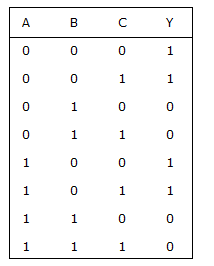
1. 0
2. 1
3. A
4. Ā

5. The circuit of the given figure realizes the function …………

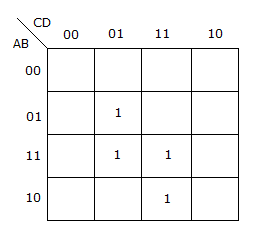
[](https://electronicspost.com/wp-content/uploads/2016/04/mcq5.png)

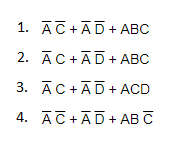
[](https://electronicspost.com/wp-content/uploads/2016/04/mcq6.png)

6.For the truth table of the given figure Y = ………….

[](https://electronicspost.com/wp-content/uploads/2016/04/mcq10.png)

1. A + B + C
2. Ā +BC
3. Ā
4. B¯

[](https://electronicspost.com/wp-content/uploads/2016/04/mcq19.png)7. For the K map in the given figure the simplified Boolean expression is ……

[](https://electronicspost.com/wp-content/uploads/2016/04/mcq20.png)

8.  In 1-to-4 demultiplexer, how many select lines are required?

a) 2  
 b) 3  
 c) 4  
 d) 5

9.  In 1-to-4 multiplexer, if C1 = 1 & C2 = 1, then the output will be \_\_\_\_\_\_\_\_\_\_\_\_

a) Y0  
 b) Y1  
 c) Y2  
 d) Y3

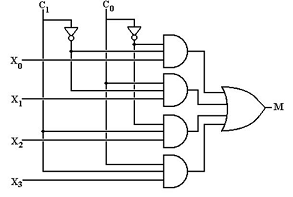
10.  How is an encoder different from a decoder?  
 a) The output of an encoder is a binary code for 1-of-N input  
 b) The output of a decoder is a binary code for 1-of-N input  
 c) The output of an encoder is a binary code for N-of-1 output  
 d) The output of a decoder is a binary code for N-of-1 output

11. For 8-bit input encoder how many combinations are possible?  
 a) 8  
 b) 2^8  
 c) 4  
 d) 2^4

12. How many inputs are required for a 1-of-16 decoder?  
 a) 2  
 b) 16  
 c) 8  
 d) 4

13. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?  
 a) Data Selector  
 b) Data distributor  
 c) Both data selector and data distributor  
 d) Demultiplexer

14. If the number of n selected input lines is equal to 2^m then it requires \_\_\_\_\_ select lines.  
 a) 2  
 b) m  
 c) n  
 d) 2n

15. In the given 4-to-1 multiplexer, if c1 = 0 and c0 = 1 then the output M is \_\_\_\_\_\_\_\_\_\_\_  
[](https://www.sanfoundry.com/wp-content/uploads/2017/06/digital-circuits-questions-answers-multiplexers-data-selectors-1-q13.png)  
 a) X0  
 b) X1  
 c) X2  
 d) X3

16.  TTL devices consume substantially \_\_\_\_\_\_ power than equivalent CMOS devices at rest.  
 a) Less  
 b) More  
 c) Equal  
 d) Very High

17. Using the transformation method you can realize any POS realization of OR-AND with only.  
 a) XOR  
 b) NAND  
 c) AND  
 d) NOR

18. The logic circuits whose outputs at any instant of time depends only on the present input but also on the past outputs are called \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  
 a) Combinational circuits  
 b) Sequential circuits  
 c) Latches  
 d) Flip-flops

19. The truth table for an S-R flip-flop has how many VALID entries?  
 a) 1  
 b) 2  
 c) 3  
 d) 4

20. What is the major difference between half-adders and full-adders?

a) Full-adders are made up of two half-adders  
 b) Full adders can handle double-digit numbers  
 c) Full adders have a carry input capability  
 d) Half adders can handle only single-digit numbers

21. The time required for a gate or inverter to change its state is called \_\_\_\_\_\_\_\_\_\_  
 a) Rise time  
 b) Decay time  
 c) Propagation time  
 d) Charging time

22. The number of full and half adders are required to add 16-bit number is \_\_\_\_\_\_\_\_\_\_  
 a) 8 half adders, 8 full adders  
 b) 1 half adders, 15 full adders  
 c) 16 half adders, 0 full adders  
 d) 4 half adders, 12 full adders

23.  The following switching functions are to be implemented using a decoder:  
 f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7)  
 The minimum configuration of decoder will be \_\_\_\_\_\_\_\_\_\_  
 a) 2 to 4 line  
 b) 3 to 8 line  
 c) 4 to 16 line  
 d) 5 to 32 line

24. How many two inputs AND and OR gates are required to realize Y = CD+EF+G?  
 a) 2, 2  
 b) 2, 3  
 c) 3, 3  
 d) 3, 2

25. The gates required to build a half adder are \_\_\_\_\_\_\_\_\_\_  
 a) EX-OR gate and NOR gate  
 b) EX-OR gate and OR gate  
 c) EX-OR gate and AND gate  
 d) EX-NOR gate and AND gate